A cascaded Couple Inductor- Reverse high step up converter integrating three-winding coupled inductor and diode-capacitor technique

Fei Li, and Hongchen Liu, Member, IEEE

Abstract—This paper introduces a cascaded high step up converter realized with a tightly coupled three-winding coupled inductor. Compared with existing high step up converters, the proposed converter features that the smaller the turns ratio is, the larger the conversion gain is. So, the name couple inductor-reverse is given to represent reverse coupled inductor principle of operation. In addition, diode-capacitor circuit is introduced to not only recycle leakage energy to output, but also further lift voltage conversion gain. This paper illustrates operation principle of the proposed converter, discusses effect of leakage inductance on voltage gain, and deduces voltage and current stresses of components. Finally, a prototype rated at 400W has been established, and experimental results verify correctness of the above theoretical analysis.

Index Terms— cascaded high step up converter, coupled inductor-reverse, reduced turns ratio, low voltage stress.

I. INTRODUCTION

As renewable energy is increasingly becoming a hot research topic, the high step-up converter is also widely employed as an interface in many industry applications, such as fuel cell system, photovoltaic system, electric vehicles, and so on[1][4]. In general, conventional boost converter can satisfy requirement in such applications[9][6]. But, some typical drawbacks exist: the voltage stress of main switch is equal to the output voltage, hence, a high voltage rating switch with high on-resistance should be used, generating high conduction losses. In addition, an extremely high duty ratio will induce large conduction losses on power devices and serious diode reverse recovery problem. Based on the above drawbacks, the conventional boost converter is not suitable for realizing high step-up voltage gain together with high efficiency. Many other techniques have been researched to achieve a high conversion ratio and avoid operating at extreme duty ratio. These techniques include the switches-capacitor techniques[7][8], switched-inductor techniques[9][10], voltage-lift techniques[11][12]. All these techniques can obtain higher voltage conversion gain than the conventional boost converter. More components, however, are needed for extremely large conversion ratio, resulting in higher cost and complex circuit.

Therefore, to achieve a high conversion ratio without operating at large duty cycle, some papers have focused on coupled inductor technique. Typical isolated flyback converter is often adopted for achieving high voltage gain by adjusting the turns ratio[13]. But, the leakage inductance may cause high voltage spikes on the switch and induce energy losses. In order to improve the problems, passive snubber circuit or active clamp circuit can be applied. But, this makes both cost and circuit high and complex. Many non-isolated converters based on coupled inductor are presented[14][19]. However, under the condition of large voltage conversion gain, the turns ratio must be very high. Using a coupled inductor with a large turn ratio also introduces several problems. For example, the leakage inductance and parasitic capacitance formed by secondary winding of the coupled inductor may cause voltage and current spikes and increase loss and noise that will dramatically degrade the system performance[20]. In order to satisfy the large high step-up applications, cascaded high step-up converters were proposed[21][22]. But, among these converters, the voltage conversion gain is approximately proportional to the turns ratio. Sometimes, the problem of high turns ratio still exists.

In this paper, a novel cascaded high step-up converter with three-winding coupled inductor and diode-capacitor structures...
is proposed. The features of the proposed converter are as follows:

1) The smaller the turns ratio is, the higher voltage conversion gain is,
2) The voltage stresses on power switch and diodes are very low, this makes low on-resistance mosfet and schottky diodes available,
3) Leakage inductance energy can be recycled to the output,
4) The cascaded structure makes voltage conversion gain higher.

II. INFLUENCE OF TURNS RATIO OF COUPLED INDUCTOR

Coupled inductor, as a popular technology, has been applied for boosting voltage gain. In general, the voltage gain can be effectively boosted by increasing the turns ratio of coupled inductor. The higher turns ratio, however, introduces some problems. The higher turns ratio is, the larger leakage inductance and parasitic capacitor are as shown in Fig.1[25][26]. In addition, the higher turns ratio make lower power density, large core and copper losses. These all degrade the converter performance. Therefore, a better solution is that find a converter with following characteristic, i.e. the smaller the turns ratio is, the larger the voltage gain is.

In order to simplify circuit analysis of the proposed converter, some assumptions are shown as follows,
1) the input inductor \( L_{in} \) is large enough so that current \( i_{in} \) keeps continuous;
2) all the capacitors are large enough so that the voltage stresses across them are constant during one switching period;
3) The diodes are ideal, and parasitic capacitor of switch \( S \) is considered;
4) Only CCM mode (both currents \( i_{in} \) and \( i_{out} \) are continuous) is considered.

Based on the above assumptions, Fig.3 shows typical waveforms of the proposed converter during one whole switching period, and equivalent circuits are shown in Fig.4. The five operating modes are described as follows.
(1) Mode I \([t_0, t_1]\). During this mode, the switch S starts to conduct. The diodes \(D_2, D_3\) and \(D_4\) are reverse biased, and diodes \(D_1\) and \(D_5\) are forward biased. The current-flow path is shown in Fig.4 (a). The currents \(i_{t_0}, i_k, i_{i_0}, i_{t_1}, i_{i_1}\) and \(i_{t_2}\) increase linearly. The currents \(i_{t_3}\) and \(i_{i_2}\) decrease linearly. The input source \(V_{in}\), input inductor \(L_m\), magnetizing inductance \(L_{m}\), and multiplier capacitor \(C_2\) are in series to provide energies to the load \(R\) and output capacitor \(C_o\). When the charging current \(i_{t_3}\) decreases to zero at \(t_1\), this mode ends.

(2) Mode II \([t_1, t_2]\). During this mode, the switch S keeps conducting. The diodes \(D_1, D_3\) and \(D_4\) are reverse biased, and diodes \(D_2\) and \(D_5\) are forward biased. The current-flow path is shown in Fig.4 (b). The input inductor \(L_m\) is charged by input source \(V_{in}\). As the capacitor \(C_1\) provides energy, the currents \(i_{t_0}, i_k, i_{i_0}\) increase linearly. In addition, the windings of coupled inductor \(N_1\) and \(N_2\), clamped capacitor \(C_c\) are in series to provide energy to the multiplier capacitor \(C_2\). The output capacitor \(C_o\) provides energy to the load \(R\). When the switch S is turned off at \(t_2\), this mode ends.

(3) Mode III \([t_2, t_3]\). During this mode, the switch S is turned off. The diodes \(D_1, D_3\) and \(D_4\) are reverse biased, and diodes \(D_2\) and \(D_5\) are forward biased. Fig.4(c) shows the current-flow path. The energies of leakage inductor \(L_{k_2}\) and \(L_{k_1}\), magnetizing inductance \(L_m\) and input inductor \(L_m\) are released to the parasitic capacitor of switch S. The multiplier capacitor \(C_2\) is still charged by the windings of coupled inductor \(N_1\) and \(N_2\), clamped capacitor \(C_c\). Meanwhile, the output capacitor \(C_o\) provides energy to the load \(R\). When the voltage stress across the parasitic capacitor of switch S is equal to the voltage stress across clamped capacitor \(C_c\) at \(t_3\), this mode ends.

(4) Mode IV \([t_3, t_4]\). During this mode, the switch S keeps off. The diodes \(D_1, D_3\) and \(D_4\) are forward biased, and diodes \(D_2\) and \(D_5\) are reverse biased. Fig.4 (d) shows the current-flow path. The capacitor \(C_1\) is charged by the input source \(V_{in}\) and input inductor \(L_m\). The clamped capacitor \(C_c\) is charged by the energies of leakage inductor \(L_{k_2}\), \(L_{k_1}\) and magnetizing inductance \(L_m\). The currents \(i_{t_0}\) and \(i_{i_0}\) decrease and current \(i_{t_1}\) increases. The input source \(V_{in}\), input inductor \(L_m\), magnetizing inductance \(L_m\) and multiplier capacitor \(C_2\) are in series to provide energies to the load \(R\) and output capacitor \(C_o\). When the charging current \(i_{t_3}\) is equal to zero at \(t_4\), this mode ends.

(5) Mode V \([t_4, t_5]\). During this mode, the switch S still keeps off. The diodes \(D_1, D_3\) and \(D_5\) are forward biased, and diodes \(D_2, D_3\) and \(D_4\) are reverse biased. Fig.4 (e) shows the current-flow path. The capacitor \(C_1\) is still charged by the input source \(V_{in}\) and input inductor \(L_m\). The input source \(V_{in}\), input inductor \(L_m\), magnetizing inductance \(L_m\) and multiplier capacitor \(C_2\) are in series to provide energies to the load \(R\) and output capacitor \(C_o\). When the switch S begins to conduct at \(t_5\), next switching period begins.

IV PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

To simplify the analysis of the proposed converter, the modes I and III are ignored. During the time period of mode II, following equations can be expressed based on Fig.4 (b),

\[ V_{in} = V_{im} \]
\[ V_{in} + L_{k_2} + L_{k_1} = N_1 V_{im} = N_1 V_{cm} = V_{c_1} \]

And the voltage stress across the multiplier capacitor \(C_2\)

\[ V_{cm} = \frac{N_1}{N_2} V_{im} + \frac{N_1}{N_2} V_{lm} = \frac{L_{k_1} + L_{k_2}}{L_m} V_{cm} \]

During the time duration of mode IV, following equation can be derived as,

\[ V_{im} + \frac{L_{k_2} + L_{k_1}}{L_m} = \frac{N_1}{N_2} V_{im} = V_{cm} = V_{c_1} \]

During the time duration of modes IV and V, following expression can be written as,

\[ V_{in} = V_{im} - V_{cm} \]
\[ V_{im} + \frac{L_{k_2} + L_{k_1}}{L_m} = \frac{N_1}{N_2} V_{im} = V_{cm} = V_{cm} = V_{cm} \]

Applying inductor volt-second balance principle to the inductor \(L_m\) and magnetizing inductor \(L_m\), following equations can be expressed as,

\[ \int_{0}^{t_5} V_{im} dt + \int_{0}^{t_5} V_{cm} dt = 0 \]
\[ \int_{0}^{t_5} V_{im} dt + \int_{0}^{t_5} V_{cm} dt = 0 \]

From equations (1)-(8), the voltage stresses across capacitors are computed as

\[ V_{cm} = \frac{1}{1 - D} \]
\[ V_{cm} = \frac{1}{1 - D} \]

The voltage across magnetizing inductance \(L_m\) during mode IV can also be written as

\[ V_{im} = \frac{V_{cm}}{1 - L_{k_2} + L_{k_1} - \frac{N_1}{N_2} \cdot \frac{1}{1 - D} \cdot \frac{1}{L_m}} \]
Substituting (9)-(12) into (6), the voltage conversion gain can be obtained as

\[
M = \frac{1}{1-D} + \frac{1}{1-D} \frac{n_2 + n_3}{n_1 - 1} \quad (14)
\]

Where \(n_1 = N_2 / N_1\) and \(n_2 = N_3 / N_1\) are the turns ratios of the coupled inductor.

The diagram of voltage gain versus duty cycle under various leakage inductance is shown in Fig.5(a). It is seen that as the leakage inductance decreases, the gain increases. When the leakage inductance is ignored, the ideal voltage conversion gain can be simplified as

\[
M = \frac{1}{1-D} + \frac{1}{1-D} \frac{n_2 + n_3}{n_1 - 1} \quad (13)
\]

Fig. 5 (a) The effect of leakage inductance on voltage gain. (b) The tendency of voltage gain curve considering the parasitic resistor.

Of course, when considering the parasitic resistor, the voltage gain is not approximately proportional to the duty cycle, the tendency of voltage gain curves is shown in Fig.5(b). As the duty cycle increases, a maximum limitation of voltage gain exists.

Fig.6 shows the relationships between the voltage gain and duty cycle in the quadratic boost converter, reference [22] converter, and the proposed converter under different turns ratio \(n_1\) (assuming that \(n_2 = 1\)). It is clear that as the turns ratio \(n_1\) is larger, the gain of proposed converter is lower than the converter in [22]. As the turns ratio \(n_2\) is small, however, the gain of the proposed converter is higher than the other converters. Therefore, the proposed converter can achieve a higher gain with less turns ratio. This is beneficial for improving performance of the proposed converter.

B. Voltage Stress Analysis

According to the operating modes in section III, the
voltage stresses of power devices can be derived by

\[
V_s = V_{D_s} = \frac{V_{in}}{(1-D)^2} = \frac{V_o (n_2 - 1)}{2n_2 - 1 + n_3}
\]

(15)

\[
V_{D_1} = \frac{V_{in}}{1-D} = \frac{V_o (n_2 - 1)(1-D)}{2n_2 - 1 + n_3}
\]

(16)

\[
V_{D_2} = \frac{DV_{in}}{(1-D)^2} = \frac{DV_o (n_2 - 1)}{2n_2 - 1 + n_3}
\]

(17)

\[
V_{D_{in}} = V_{D_{in}} = \frac{V_{in}}{(1-D)^2} = \frac{V_o (n_2 + n_1)}{2n_2 - 1 + n_3}
\]

(18)

The Fig. 7 shows the normalized voltage stresses comparison of components among different converters.

The Fig.7 shows the normalized voltage stresses comparison of different components between the quadratic boost converter, reference [22], and the proposed converter. As shown in Fig.7 (a) and (b), in the quadratic boost converter, the maximum voltage stress of the main switch and diodes is constant, and equal to the output voltage. As shown in Fig.7, when the turns ratio \( n_2 \) increases, the voltage stresses on the switch, diode and capacitor in the reference [22] respectively decrease, increase and increase. However, the voltage stresses on the switch, diode and capacitor in the proposed converter have a completely inverse variation. This characteristic is absolutely different from other high step up dc/dc converters. It is beneficial for improving the performance of the proposed converter. In addition, based on inconsistent change, a designed compromise should be made.

C. Current Stress Analysis

As the modes I, III are very transient, thus, they are reasonably neglected. Other parasitic factors are also ignored. The simplified waveforms are shown in Fig.8.

According to the current balance law, average currents of the output diode \( D_o \) and diode \( D_1 \) in its turn on condition are,

\[
I_{D_{o}[t_4-t_5]} = I_o/(1-D)
\]

(19)

\[
I_{D_{1}[t_4-t_5]} = I_o/D
\]

(20)

Based on the charge balance principle of capacitor \( C_o \), the time interval \( t_{24} \) and \( t_{45} \) can be derived as

\[
t_{24} = t_s - \frac{2(1-D)(n_2 - 1)}{2n_2 + n_3 - 1} T_s
\]

(21)

\[
t_{45} = \frac{(1-D)(n_2 + n_1)}{2n_2 + n_3 - 1} T_s
\]

(22)

According to the current balance law, average current of the clamped diode \( D_3 \) in its turn on condition is:

\[
I_{D_{3}[t_2-t_4]} = \frac{I_o (2n_2 + n_3 - 1)}{2(1-D)(n_2 - 1)}
\]

(23)

During the time interval \([t_2,t_4]\), while using KCL(Kirchhoff’s Current Law), at junction points of the primary side \( N_2 \) of the coupled inductor, secondary side \( N_1 \) of the coupled inductor, and third side \( N_3 \) of the coupled inductor, the average current of the leakage inductor \( L_{k2} \) can be written as

\[
I_{k2[t_2-t_4]} = 2I_o/(1-D)
\]

(24)

According to the magnetic flux conservation principle and
Fig. 8. Following expression can be deduced

\[ N_2 I_{t_2[t_2,t_1]} - N_1 I_{t_1[t_1,t_2]} - N_3 I_{t_3[t_3,t_2]} \]

\[ = N_2 I_{t_2[t_2,t_1]} - N_1 I_{t_1[t_1,t_2]} + N_3 I_{t_3[t_3,t_2]} \]  \hspace{1cm} (25)

Meanwhile,

\[ I_{t_3[t_3,t_2]} = I_{t_2[t_2,t_1]} + I_{t_1[t_1,t_2]} \]  \hspace{1cm} (26)

Collecting the terms, \( I_{t_3[t_3,t_2]} \) can be computed as

\[ I_{N_3[t_3,t_2]} = I_o \frac{D}{2} \left[ 2n_2 + n_3 + 1 \right] + \frac{2n_3(n_1 - n_3)}{(1 - D)^2(n_2 - 1)^2} \]  \hspace{1cm} (27)

Based on the ideal gain expression, during the time interval \([t_1,t_2]\), average current of the diode \(D_2\) can be written as

\[ I_{D_2[t_2,t_1]} = \frac{D}{2} \left[ 2n_2 + n_1 - 1 \right] \]  \hspace{1cm} (28)

Therefore, total average current through switch S during the time interval \([t_1,t_2]\) can be obtained as

\[ I_{S[t_1,t_2]} = \frac{D}{2} \left[ 2n_2 + n_1 - 1 \right] \]  \hspace{1cm} (29)

Then, the RMS value of switch S is,

\[ I_{RMS} = \frac{1}{T_s} \int_{T}^{0} \left( I_{S[t_1,t_2]} - 0.5 \Delta I + \frac{\Delta I}{DT_s} t \right)^2 \]  \hspace{1cm} (30)

Where, \( K \) is the coefficient of inductor current ripple

\[ \Delta I = K I_{I_2[t_2,t_1]} \].

D. Performance Comparison Between the Proposed Converter and Other Converters

For the sake of performance comparing, another two three-winding coupled inductor high step-up converters are introduced \([23]-[24]\). In order to fair compare, the turns ratio of coupled inductor is the same: \( n_1 = 1.5 \), \( n_3 = 1.5 \). Table I summarizes the voltage conversion gain, switch stresses, maximum diode stresses, maximum capacitor stresses, and numbers of components.

From the view of numbers of components, the numbers of components in the proposed converter is almost the same as that in \([24]\). The cost between them is almost equal. Meanwhile, the numbers of components in the proposed converter is larger than that in \([23]\). This increases the cost of the proposed converter. However, as shown in Fig. 9(a) and (b), the voltage gain and switch stresses in the proposed converter have advantages. In Fig. 9(a), it turns out that the voltage gain of the proposed converter is far higher than that of other converters as the turns ratio is small. Meanwhile, Fig. 9(b) reveals that the voltage stress of switch of the proposed converter is lower than other converters. It is a very attractive feature. This makes the low voltage rated MOSFET available and improves the performance of the proposed converter. In Fig. 9(c), maximum voltage stresses of the diodes in the proposed converter is constant. But, as the duty cycle increases, maximum voltage stresses of the diodes in other converters also increase. Fig. 9(d) depicts the curves of maximum capacitor voltage stresses. The maximum voltage stresses of capacitor among them are nearly equal.

E. Advantage and Disadvantage of the Proposed Converter

In the proposed converter, voltage gain formula is different from other converters. The voltage gain formula combines both square feature and inverse ratio feature of the turns ratio. The two features can reduce the duty cycle, winding turns, voltage stress and coupled inductor volume and so on when operating at the same condition. Of course, the disadvantage of the proposed converter is also obvious. The numbers of components are very large. For the 3-winding coupled inductor, 3 windings can be enwinded in one magnetic core, this part almost does not add the cost. The four diode models are schottky diode and the output diode model is the SiC diode. The SiC diode adds the cost, but other common model can be used as the output diode. The numbers of capacitors are large, but the capacitor \( C_2 \) and \( C_1 \) have low voltage stresses. The cost of capacitors mainly is determined by other two capacitors. Therefore, the overall cost does not increase a lot compared with other high step up converters. Last, a compromise must be made in the high step up application.

V DESIGN GUIDELINE

A. Input Inductor Design

The input inductor can not only smooth input current of the proposed converter, but also filter the higher harmonics. The main design criterion of the input inductor is to control the input current ripple to a reasonable range. So,

When the switch is closed, the input inductor is charging, relevant equation is

\[ \Delta i = \frac{V_n}{f} \frac{D}{L_{in}} \]  \hspace{1cm} (31-1)

According to power balance, the average input current is derived as

\[ I_{in} = \frac{P_o}{V_{in}} \]  \hspace{1cm} (31-2)
The maximum input current ripple is
\[ \Delta i \leq I_i K_i \]  

(31-3)

Lastly, combining (a), (b) and (c), the input inductance is written as
\[ L_i \geq \frac{V_{in}^2 f}{D f^2 K_i P_i} \]  

(31)

Where \( P_i \) is the output power, \( V_{in} \) is the input voltage,

\[ K_i \] is the input current ripple coefficient.

B. Turns Ratio Design of Coupled Inductor

The turns ratio of coupled inductor affects the voltage stress, current stress and so on. Therefore, it is critical to give a reasonable design equation.

<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain</td>
<td>((1 + n_i) + \frac{1 + Dn_2}{1 - D})</td>
<td>(n_2 + \frac{2 - D + n_1}{1 - D})</td>
<td>(\frac{1}{1 - D} \cdot \frac{2n_i + n_3 - 1}{n_2 - 1})</td>
</tr>
<tr>
<td>Voltage stress of active</td>
<td>(V_o)</td>
<td>(V_o)</td>
<td>(n_2 - 1) (V_o)</td>
</tr>
<tr>
<td>switches</td>
<td>((1 + n_i)(1 - D)+1 + Dn_2)</td>
<td>(2 - D + (1 - D)n_1 + n_3)</td>
<td>(2n_2 - 1 + n_1)</td>
</tr>
<tr>
<td>Maximum voltage stress of</td>
<td>((1 + n_i)V_o)</td>
<td>((1 + n_i)V_o)</td>
<td>((1 + n_i)V_o)</td>
</tr>
<tr>
<td>diodes</td>
<td>((1 + n_i)(1 - D)+1 + Dn_2)</td>
<td>(2 - D + (1 - D)n_2 + n_3)</td>
<td>((n_2 - 1)(2n_2 - 1 + n_1))</td>
</tr>
<tr>
<td>Maximum voltage stress of</td>
<td>((1 + n_i)(1 - D)V_n)</td>
<td>((1 + n_i)(1 - D)V_n)</td>
<td>((n_2 - 1)(2n_2 - 1 + n_1))</td>
</tr>
<tr>
<td>capacitors</td>
<td>((1 + n_i)(1 - D)+1 + Dn_2)</td>
<td>(2 - D + (1 - D)n_2 + n_3)</td>
<td>((n_2 - 1)(2n_2 - 1 + n_1))</td>
</tr>
<tr>
<td>Numbers of capacitors</td>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Numbers of diodes</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

Fig.9 (a) Voltage gain comparison. (b) Switch voltage stresses comparison. (c) Diode voltage stresses comparison. (d) Capacitor voltage stresses comparison

Based on the equations (14), (15), (16), (17) and (18), as the \( n_i \) increases, the voltage stresses of power devices decrease, as the \( n_i \) increased, the voltage stresses of power devices also decrease. Therefore, a proper \( n_i \) can be obtained when the duty cycle and \( n_i \) is designed, which is given by
\[ n_2 = \frac{n_1 - 1 + M(1 - D)}{M(1 - D)^2 - 2} \]  

(32)

C. The Capacitors Design

A decent clamp capacitor value can effectively limit the voltage spike of the MOSFET. Therefore, based [15], the clamp capacitor can be computed as
\[ 2\pi \sqrt{(L_{i1} + L_{i2})} C_c \geq 0.5 \cdot (1 - D) f_s \]  

(33-1)

Thus,
\[ C_c \geq \frac{(1 - D)^2}{\pi^2 f_s^2 (L_{i1} + L_{i2})} \]  

(33)

Where \( f_s \) (1/T_s) represents switching frequency.

Other three capacitors limit voltage ripple to a reasonable range. Thus, according to the charge balance principle,
\[ CAV' \geq Q = I^* \Delta t \]  

(34-1)

Thus, the capacitors can be respectively represented as
\[ C_{i1} \geq \frac{V_o}{2} \frac{D f_s}{f_s} \Delta V_P \]  

(34)

\[ C_{i2} \geq \frac{V_o}{R \Delta V_P} \]  

(35)
In addition, according to the part C. Current stress analysis, the average current of winding $N_2$ is derived as

$$I_{\text{avg}} = I_s \left( \frac{2n_2 + n_1 - 1}{(1 - D)} \frac{1}{(n_2 - 1)} - \frac{1}{D} \right)$$  \hspace{1cm} (36-1)

Therefore,

$$C_1 \Delta V_s \geq I_{\text{avg}} D / f_s$$  \hspace{1cm} (36-2)

$$\Rightarrow C_1 \geq \frac{V_s D}{2n_2 + n_1 - 1} \frac{1}{(1 - D)} \frac{1}{(n_2 - 1)} - \frac{1}{D}$$  \hspace{1cm} (36)

Where $\Delta V_s$, $\Delta V_1$, and $\Delta V_2$ are the voltage ripple.

VI EXPERIMENTAL RESULTS

<table>
<thead>
<tr>
<th>Parameter/Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power rating $P_o$</td>
<td>400W</td>
</tr>
<tr>
<td>Input voltage $V_{in}$</td>
<td>38V</td>
</tr>
<tr>
<td>Output voltage $V_o$</td>
<td>380V</td>
</tr>
<tr>
<td>Capacitors</td>
<td>CBB capacitor $C_2=4.4 \mu F$, $C_3=8.8 \mu F$; Electrolytic capacitor $C_1=470 \mu F$</td>
</tr>
<tr>
<td>Coupled inductor</td>
<td>EE55, $N_1 : N_2 : N_3 = 30 : 16 : 16$; $L_{c1} \approx 508 \mu H$, $L_{c2} \approx 7.4 \mu H$</td>
</tr>
<tr>
<td>Input inductor</td>
<td>$L_{i1} \approx 2.6 \mu H$, $L_{i2} \approx 3.1 \mu H$, $\approx 160 \mu H$</td>
</tr>
<tr>
<td>Output capacitors $C_o$</td>
<td>Electrolytic capacitor $470 \mu F$</td>
</tr>
<tr>
<td>Switching frequency $f_s$</td>
<td>50kHz</td>
</tr>
<tr>
<td>Switch S</td>
<td>IRFP4568</td>
</tr>
<tr>
<td>Diodes</td>
<td>$D_1$, $D_2$, $D_3$, $D_4$ VF30200, $D_5$ IDH086G65C5</td>
</tr>
</tbody>
</table>

To verify effectiveness of the theoretical analysis, a prototype circuit of the proposed converter is built and tested. The parameters of the prototype are described in Table II. The key waveforms are shown in Fig.10 and Fig.11.

Fig.10 shows the current stresses of the proposed converter. Fig. 10 (a) shows driver signal of the switch $S$, the current waveforms of primary side current $i_{c1}$ and secondary winding current $i_{c1}$. Fig. 10 (b) and (c) show the third winding current $i_{c3}$, diode currents $i_{D0}$ and $i_{D1}$, and input current $i_n$. It is clear that the input current $i_n$ is continuous. Fig. 10 (d) and (e) show the currents through switch and diode $D_1$. They are agreed well with the theoretical analysis.

Table III The comparison of experimental value and theoretical value of Mosfet RMS current

<table>
<thead>
<tr>
<th>S Duty cycle</th>
<th>Theoretical value</th>
<th>Experimental value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>13.8</td>
<td>12.6</td>
</tr>
<tr>
<td>0.4</td>
<td>17.1</td>
<td>17</td>
</tr>
<tr>
<td>0.5</td>
<td>22</td>
<td>21.6</td>
</tr>
</tbody>
</table>

In order to demonstrate the correctness of the equation (30), the experimental value and computed value of RMS current is shown in Table III. Because of the measuring error, approximate deduction, the difference between the computed value and experimental value exists. In addition, equation (30) only provides a reference for choosing MOSFET. It is not exactly the same as the experimental values.

Fig.11 shows the voltage stresses of the proposed converter. Fig. 11 (a) shows the driver stress and voltage stress of the switch $S$, and voltage stresses on the diodes. The voltage stress of switch $S$ is low so that the low on-resistance mosfet can be used. Meanwhile, the voltage stresses on the diodes are low, which makes schottky diode available. Thus, this improves the performance of the proposed converter. Fig. 11
(b) and Fig. 11 (c) show the voltage stresses on the diodes. The voltage stresses on diodes $D_1$ and $D_2$ are lower than the output voltage. The voltage stress on diode $D_3$ is low so that the Schottky diode is available. Fig. 11 (d) shows the voltage stresses across the capacitors $C_1$, $C_2$ and $C_3$. The experimental waveforms are agreed well with the theoretical analysis.

The measured efficiency comparison at different loads and input voltages between the proposed converter and the converter in [22] is shown in Fig.12 (a). As can be seen, when input voltage of the proposed converter is 38V, efficiency of the proposed converter is improved than that of the converter in [22] as the load is lighter. Meanwhile, it can be seen that maximum efficiency of the proposed converter is close to 96%. In addition, as the input voltage increases, the efficiency of the proposed converter is increased. Fig.12 (b) shows the proportion of the loss. The diode loss is large, and should be further improved. Fig.12(c) shows the experimental prototype.

VII CONCLUSION

For the high step-up applications, a novel high voltage gain converter is introduced in this paper, which combines a quadratic boost converter with three-winding coupled inductor and diode-capacitor techniques. The diode-capacitor circuit not only lifts the voltage conversion gain, but also recycled the leakage energy to the output. The three-winding coupled inductor-reverse makes the smaller turns ratio available implementing the high voltage conversion gain. Due to cascaded structure, a smaller duty cycle can produce a high conversion gain. The voltage stresses on the power switch and diodes are very low, which makes the low on resistance mosfet and Schottky diodes available. The efficiency is improved efficiently.

![Image](image_url)

(c)

Fig.12 (a) The measured efficiency curves. (b) Calculated portion of loss. (c) Experimental prototype

REFERENCES

[13] Yan Deng, Qiang Rong, Wuhua Li, YiZhao, Jianjiang Shi and Xiangning


Fei Li received the B.S. degree in electrical engineering from Hei Longjiang University, Harbin, China, in 2011, and the M.S. degree in electrical engineering from Harbin Institute of Technology (HIT), Harbin, in 2013. He is currently working toward the Ph.D. degree in power electronics and electrical drives in the School of Electrical Engineering and Automation, HIT.

His current research interests include DC/DC topology and nonlinear dynamics in power electronics.

Hongchen Liu received the B.S. in electrical engineering from Northeast Agricultural University, Master and Ph.D degrees in electrical engineering from Harbin Institute of Technology (HIT), Harbin, China, in 2001, 2003, and 2007, respectively.

In 2009, he joined the Department of Electrical Engineering, HIT as a Lecturer, where he has been an Associate Professor of electrical engineering since 2012. From 2008 to 2012, he was a Postdoctoral Fellow in Measuring and controlling technology and instrument specialty. He has authored more than 30 technical papers published in journals and conference proceedings. His current major research interests include DC/DC converter and inverter in photovoltaic system, Matrix converter and nonlinear dynamics in power electronics.